What is claimed is:

1. A semiconductor device comprising:

clock buffer means for receiving and buffering an external clock signal and then outputting an internal clock;

clock enable buffer means for comparing a reference voltage having a constant potential with a clock enable buffer signal and then enabling the clock buffer means; and

clock enable signal latch means for enabling the clock enable buffer means using the clock enable buffer signal after a power-up signal is inputted.

2. The semiconductor device as recited in Claim 1, further comprising:

clock enable signal timing control means for passing the clock enable signal to the clock buffer in response to the enable signal or outputting a delayed clock enable signal to the clock buffer by delaying the clock enable signal for a predetermined time.

3. The semiconductor device as recited in Claim 2, wherein the clock enable signal latch means includes:

a first clock enable signal latch unit which is enabled according to the power-up signal to transfer the clock enable signal and is disabled according to an enable signal; and

a second clock enable signal latch unit which enables

the clock buffer means and outputs the enable signal to disable the first clock enable signal latch unit using an output signal from the first clock enable signal latch unit.

4. The semiconductor device as recited in Claim 3, wherein the first clock enable signal latch unit includes:

a NAND gate receiving the power-up signal and the enable signal;

a first PMOS transistor which has a gate receiving the clock enable buffer signal and is connected to the power voltage;

a first NMOS transistor which has a gate receiving the clock enable buffer signal and is connected to the first PMOS transistor;

a second NMOS transistor which has a gate receiving an output signal from the NAND gate and is connected to both the first NMOS transistor and a ground voltage level;

a second PMOS transistor which has a gate receiving the output signal from the NAND gate and is connected to both the power voltage; and

a first inverter connected between the first NMOS transistor and the second PMOS transistor in order to invert a voltage level on the common node of the first NMOS transistor and the first PMOS transistor.

5. The semiconductor device as recited in Claim 4, wherein the second clock enable signal latch unit includes:

a third PMOS transistor which has a gate receiving power-up signal and is connected to the power voltage;

a fourth PMOS transistor which has a gate receiving an output signal from the first inverter and is connected to the third PMOS transistor;

a third NMOS transistor which has a gate receiving the output signal from the first inverter and is connected to both the fourth PMOS transistor and the ground voltage level; and

a second inverter to invert a voltage level on a common node of the fourth PMOS transistor and the third NMOS transistor.

6. The semiconductor device as recited in Claim 3, wherein the clock enable signal timing control means includes:

a clock enable signal path selection unit which passes the first control signal to the clock signal latch unit or outputs a delayed signal to the clock signal latch unit by delaying the first control signal; and

a path controller to control the transfer path of the first control signal on the clock enable signal path selection unit in response to the enable signal.

7. The semiconductor device as recited in Claim 6, wherein the clock enable signal path selection unit includes:

a first delayer to delay the first control signal;

a first transfer gate to transfer an output of the

first delayer to an output terminal; and

a second transfer gate to directly transfer the first control signal to the output terminal.

8. The semiconductor device as recited in Claim 7, wherein the path controller includes:

a first PMOS transistor which has a gate receiving the enable signal;

a second PMOS transistor which has a gate receiving an output signal of the clock enable signal path selection unit and is connected to the first PMOS transistor;

a first NMOS transistor which has a gate receiving the output signal of the clock enable signal path selection unit and is connected to the second PMOS transistor and the ground voltage level;

a first inverter to invert a voltage level on the common node of the second PMOS transistor and the first NMOS transistor and to produce a first turn-on signal turning on the second transfer gate;

a second inverter to invert an output signal of the first inverter and to produce a second turn-on signal turning on the second transfer gate;

a second delayer which is connected to the second inverter to and produces a third turn-on signal turning on the first transfer gate; and

a third delayer which is connected to the first inverter to and produces a third turn-on signal turning on the

first transfer gate.

9. The semiconductor device as recited in Claim 7, wherein the clock enable signal path selection unit further includes:

an inverter for inverting the power-up signal; and

an NMOS transistor for receiving an output of the inverter and connecting an input terminal of the inverter to a ground voltage level.

10. The semiconductor device as recited in Claim 8, wherein the path controller further includes:

a third inverter connected to a common node of the second PMOS transistor and the first NMOS transistor; and

a third PMOS transistorl having a gate to receive an output of the third inverter and being connected to the common node of the second PMOS transistor and the first NMOS transistor.

11. The semiconductor device as recited in Claim 1, wherein the clock enable buffer means includes:

first and second NMOS transistors which have gates receiving the reference voltage and the clock enable buffer signal, respectively;

a third NMOS transistor which has a gate receiving the enable signal and is connected to the first and second NMOS transistors and to a ground voltage level;

a first PMOS transistor which has a gate connected to the first NMOS transistor in a diode connection and is connected to a power voltage;

a second PMOS transistor which is connected to the power voltage and the NMOS transistor to form a current mirror together with the first PMOS transistor;

a third PMOS transistor which has a gate receiving the enable signal and is connected to the first NMOS transistor and the power voltage;

a fourth PMOS transistor which has a gate receiving the enable signal and is connected to the second NMOS transistor and the power voltage; and

an inverter for inverting an output signal from the common node of the second PMOS transistor and the second NMOS transistor and outputting a control signal to control the clock buffer means.